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10/612,934	07/07/2003	Takehiro Shimizu	H-1098	6928

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,934	SHIMIZU ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,9 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,9 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. DETAILED ACTION

2. Claims 1, 8, 9 and 12 have been examined.

3. Acknowledgement of papers filed: amendments and remarks on June 15th, 2006. These papers filed have been placed on record.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Data Processing Device with a Spare Field in the Instruction Indicating Whether an Instruction is a Branch Instruction.

Claim Objections

5. Objections have been withdrawn.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In particular, claim 12 discloses a carry bit being stored in the spare field. Claim 1, on which claim 12 is dependant, discloses information regarding to whether or not an instruction is a branch instruction being stored in the spare field. These appear to be to contradictory embodiments. In fact, Applicant appears to make this same argument in the Remarks by stating "the carry bit...does not provide an indication of whether or not an instruction is a branch instruction or not" (page 12 and 13). In case Applicant does believe that a carry bit does disclose an indication of whether or not an instruction is a branch, the previous rejection has been maintained.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Talcott (U.S. Patent No. 5,964,869).

Regarding claim 1, Talcott discloses a data processing device which decodes (col 5 liens 39-40) and executes instructions (col 5 lines 62-64) containing a spare field (TBAT referene 208), comprising:

An instruction cache memory (col 5 line 39).

A predecode-processor (col 8 lines 8-13) which decodes operation codes contained in first fields of each of said instructions to generate a piece of information (col 8 lines 8-13), said information representing whether said instruction is a branch instruction or not (col 8 lines 11-13), and transfers information as said spare field of each of said instructions (col 11 lines 10-14); and

Note that the one-to-one correspondence allows the predecode bits to be a portion of the instruction or "spare field".

An instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory (col 3 lines 35-49),

Wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field (col 8 lines 8-13).

Regarding claim 8, Talcott discloses the data processing device according to claim 1, wherein the instruction flow comprises:

A queuing buffer temporarily storing instructions loaded from said instruction cache memory (col 8 lines 3-7); and

A target buffer which holds an address of said branch destination (col 3 lines 41-45), said instruction of said address of said branch destination (col 4 lines 61-62),

Note that the elements of memory that contain this information are considered to be the "target buffer".

Wherein said instruction flow unit divides one branch operation into a prepare target instruction and a branch procedure instruction (see below),

Wherein said prepare target instruction commands calculating of said address of said branch destination and fetching of said instruction of said branch destination (col 3 lines 41-45),

Wherein said branch procedure instruction commands branch condition checks and branch procedures (col 5 lines 58-62).

Note that the Computer Science definition of the American Heritage College Dictionary, 4th Edition states that an instruction is "a sequence of bits that tells a central processing unit to perform a particular operation and can contain data to be used in that operation". The branch instruction completes both the operations of the "branch procedure instruction" and the "prepare target instruction"; therefore, it is considered to be split into those instructions.

Regarding claim 9, Talcott discloses the data processing device according to claim 8, wherein said instruction flow unit issues commands to load said instruction of said branch destination and said following address from said target buffer when said

instruction flow unit determines that said instruction is a branch procedure instruction according to said information of said queuing buffer (col 5 lines 52-57).

1. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Augsburg et al. (U.S. Patent No. 6,948,053) hereinafter referred to as Augsburg.

2. As per claim 1, Augsburg discloses a data processing device, capable of decoding and executing instructions, comprising: a cache memory (Fig. 2 instruction cache 203) where said instructions are held, wherein said instructions each contain a spare field (Fig. 6 bit 601), and wherein said cache memory holds information which is generated according to predecoding of instructions in a first corresponding area corresponding to said spare field. (Col. 3 lines 18-23) *The examiner asserts that field 601 is a spare field. Before an instruction is predecoded, nothing exists in the bit following the displacement of a conditional branch instruction (as in Fig. 5), rendering the bit field a spare field.*

Augsburg also discloses a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and transfers the information as said spaire field of each of said instructions.

Note that the carry bit is considered to be an indication of whether or not an instruction is a branch instruction because a branch is the only instruction that utilizes

that carry bit. Consequently, if the spare instruction contains a carry bit, the instruction is a branch instruction; otherwise, the instruction is not a branch instruction.

10. As per claim 12, Augsburg discloses the data processing device according to claim 10, wherein to handle relative branch instructions of program counters with n bit displacements, said processor adds information of n lower bits of addresses of said program counters for displacements of said first fields in an adding operation, and wherein added results by said processor are held in said second corresponding area of said cache memory, and wherein carry information of said adding operation is held in said first corresponding area. (Col. 5, lines 46-64)

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Talcott.

Regarding claim 12, Talcott discloses the data processing device according to claim 1.

Talcott fails to disclose the use of relative branch instructions that require an add to the current program counter.

Examiner asserts that relative branch instructions are extremely common in processing units similar to those of Talcott.

The use of a relative branch instruction is a common and well-known technique of limiting the required number of bits utilized in an instruction. An absolute branch requires all the address bits to be present in the instruction. This technique requires extra hardware, extra power, extra space, and perhaps a detriment to speed.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the system of Talcott to utilize relative branch instructions that require the relative displacement to be added to the program counter.

Note that the conflicting limitations with regard to the objection above are ignored in this claim.

3. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augsburg in view of Nishimukai, in further view of Irie et al. (U.S. Patent No. 6,499,712) hereinafter referred to as Irie.

4. As per claim 8, Augsburg in view of Nishimukai disclose the data processing device according to claim 1, further comprising:

a queuing buffer temporarily storing instructions loaded from said instruction cache memory (Augsburg Fig. 2 decode unit 204) *The examiner asserts that an instruction is temporarily stored in the decoder after being fetched from the instruction cache*;

Augsburg fails to disclose said controlling means commands fetching an instruction of a branched place, when it determines that said instruction is a branch instruction according to said information in said first corresponding area of said cache memory.

Nishimukai discloses fetching an instruction of a branched place, when it determines that said instruction is a branch instruction. (Col. 2 line 65 – col. 3 line 9)

Nishimukai discloses that his invention "can shorten the branch instruction executing time" (Col. 1 line 13-14), which is a desired effect in Augsburg's invention.

It would have been obvious to one of ordinary skill in the art at the time of invention to have combined Nishimukai's method of fetching a branch target instruction upon decoding a conditional branch instruction for the benefit of shortened branch instruction processing time. Consequently, Augsburg/Nishimukai discloses the following:

and a target buffer (Nishimukai's index and data fields inside his associative memory) which holds an address of said branched place, said instruction of said branched place, and a following address of said address of said branched place, *The*

examiner asserts that in the example beginning in Nishimukai's col. 5, instruction 10 is the instruction of said branched place and its address and the address of instruction 11 are both stored in index fields of associative memory 10. Instruction 11's address is a following address of instruction 10's.

Augsburg and Nishimukai fail to disclose dividing one branch operation into a prepare target instruction and a branch procedure instruction, wherein said prepare target instruction commands the calculations of said address of said branched place and fetching of said instruction of said branched place, wherein said branch procedure instruction commands branch condition checks and branch procedures.

Irie discloses dividing one branch operation into a prepare target instruction and a branch procedure instruction, wherein said prepare target instruction commands the calculations of said address of said branched place and fetching of said instruction of said branched place, wherein said branch procedure instruction commands branch condition checks and branch procedures. (Col. 9 lines 40-56)

Irie discloses low-penalty branching (Col. 9 lines 40-43) which is well-known in the art to decrease pipeline stalls and processing time. Increased processing performance is a goal of Augsburg's and Nishimukai's inventions.

It would have been obvious to one of ordinary skill in the art at the time of invention to include Irie's method of splitting branch instructions into prepare-target instructions and branch operation instructions in Augsburg's decode unit for the benefit of reducing branching penalties, and therein increasing processing performance.

5. As per claim 9, Augsburg in view of Nishimukai and Irie disclose the data processing device according to claim 8, wherein said controlling means issues commands to load said instruction of said branched place and said following address from said target buffer when said controlling means determines that said instruction is a branch procedure instruction according to said information of said queuing buffer which was loaded from the spare field of each instruction of said cache memory. *The examiner asserts that when the decoder has determined the branch target address using Augsburg's carry bit, it can fetch Nishmukai's instruction 10 (Col. 8 lines 7-14) and use the address of instruction 11 to load instruction 11 (Col. 8 lines 34-35).*

Response to Arguments

13. Applicant's arguments with respect to claims 1, 8, 9 and 12 have been considered but are moot in view of the new ground(s) of rejection under Talcott.

The Information Disclosure Statement has been considered.

The title objection remains; see suggestion above.

Figure 10, as amended, does overcome the objection in the previous action.

The objections to the specification, with exception of the title, have been withdrawn.

Examiner agrees that the claim objection with regards to claim 7 has been rendered moot.

Applicant states:

"Examiner asserts that the encoding logic unit of Augsburg as shown in Fig. 2, item 202, is equivalent to the predecode-processor of the present invention. This is clearly incorrect in that an encoding logic unit provides encoding functions, when the predecode processor of the present invention provides decoding functions."

Examiner disagrees. The encoding logic completes the claimed functionality of the predecode-processor; therefore, a predecode-processor element exists in this encoder. The presence of additional functionality does not contradict the equivalence of these two elements.

Applicant states:

Further,...the decode/selecting logic unit of Augsburg may be configured to determine if the instruction is a relative branch instruction by reading the operation code of the instruction. This is quite different from the present invention, where the predecode-processor decodes operation codes contained in first fields of the instructions to generate a piece of information, the information representing whether or not the instruction is a branch instruction."

Examiner disagrees. These appear to be quite equivalent in regards to the claim language. Both review codes of the instruction and gain information as to whether or not an instruction is a branch instruction.

Note that further discussion over whether or not a carry bit indicates whether or not an instruction is a branch instruction is discussed with respect the rejection of claim 12 under 35 USC 112.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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